

SEMICONDUCTOR DEVICE HAVING A THIN FIN AND
RAISED SOURCE/DRAIN AREAS

TECHNICAL FIELD

[0001] The present invention relates to semiconductor devices and methods of manufacturing semiconductor devices. The present invention has particular applicability to double-gate devices.

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The

FinFET structure may also be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

[0005] Implementations consistent with the present invention provide a FinFET device with a thin fin and raised source/drain areas. By having raised source/drain areas, the source/drain resistance of the FinFET device may be reduced.

[0006] Additional advantages and other features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

[0007] According to the present invention, the foregoing and other advantages are achieved in part by a semiconductor device that includes a substrate, an insulating layer, a fin, a source region and a drain region. The insulating layer is formed on the substrate and the fin is formed on the insulating layer. The source region is formed on the insulating layer adjacent a first side of the fin and the drain region is formed on the insulating layer adjacent a second side of the fin opposite the first side. The source and drain regions have a greater thickness than the fin.

[0008] According to another aspect of the invention, a method of manufacturing a semiconductor device is provided. The method includes forming a first mask over a silicon on insulator (SOI) wafer, where the SOI wafer includes a conductive layer on an insulating layer that is formed on a substrate. The method also includes etching a portion of the conductive layer to form a fin structure. The method further includes forming a source region and drain region adjacent respective ends of the fin structure, forming a second mask over the source region and drain region and etching the fin structure to reduce the width and thickness of the fin structure.

The method also includes depositing a gate material over the fin structure and patterning and etching the gate material to form a gate electrode.

[0009] According to a further aspect of the invention, a semiconductor device that includes a substrate, an insulating layer, a conductive fin, a source region and a drain region is provided. The insulating layer is disposed on the substrate and the conductive fin is formed on the insulating layer, where the conductive fin has a first end and a second end. The source region is formed adjacent the first end of the conductive fin and the drain region is formed adjacent the second end of the conductive fin. The source and drain regions each have a greater thickness than the conductive fin in the channel region of the semiconductor device.

[0010] Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

[0012] Fig. 1 is a cross-section illustrating exemplary layers that may be used for forming a fin in accordance with an embodiment of the present invention.

[0013] Fig. 2 is a cross-section illustrating the etching of the semiconductor device of Fig. 1 to form a fin in accordance with an exemplary embodiment of the present invention.

[0014] Fig. 3 is a top view illustrating the semiconductor device of Fig. 2 in accordance with an exemplary embodiment of the present invention.

[0015] Fig. 4 is a top view illustrating the formation of a mask on the semiconductor device of Fig. 3 in accordance with an exemplary embodiment of the present invention.

[0016] Fig. 5 is a top view illustrating the thinning of the fin of the semiconductor device of Fig. 4 in accordance with an exemplary embodiment of the present invention.

[0017] Fig. 6 is a cross-section illustrating the thinned fin of the semiconductor device of Fig. 5 in accordance with an exemplary embodiment of the present invention.

[0018] Fig. 7 is a cross-section illustrating the formation of a gate dielectric on the semiconductor device of Fig. 6 in accordance with an exemplary embodiment of the present invention.

[0019] Fig. 8A is a cross-section illustrating the formation of a gate on the device of Fig. 7 in accordance with an exemplary embodiment of the present invention.

[0020] Fig. 8B is a top view illustrating an exemplary double-gate device formed in accordance with an exemplary embodiment of the present invention.

[0021] Figs. 9A-9H are exemplary cross-sections and top views illustrating the formation of asymmetric gates in accordance with another embodiment of the present invention.

[0022] Figs. 10A-10F are cross-sections and top views illustrating the formation of a asymmetric gates in accordance with a further embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0024] Implementations consistent with the present invention provide FinFET devices and methods of manufacturing such devices. The FinFET devices formed in accordance with the present invention include a thin fin with raised source/drain areas formed adjacent the fin. The resulting FinFET devices have reduced source/drain resistance as compared to conventional FinFET devices.

[0025] Fig. 1 illustrates the cross-section of a semiconductor device 100 formed in accordance with an exemplary embodiment of the present invention. Referring to Fig. 1, semiconductor device 100 may include a silicon on insulator (SOI) structure that includes a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 on the buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

[0026] In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1500 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 200 Å to about 1000 Å. Silicon layer 130 is used to form a fin for a FinFET device, as described in more detail below.

[0027] In alternative implementations consistent with the present invention, substrate 110 and layer 130 may comprise other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

[0028] Next, a photoresist material may be deposited and patterned to form a photoresist mask 140 for subsequent processing, as illustrated in Fig. 1. The photoresist may be deposited and patterned in any conventional manner. In an exemplary implementation, the photoresist mask 140 may be trimmed to a width ranging from about 200 Å to about 500 Å.

[0029] Semiconductor device 100 may then be etched to form the fin structure. In an exemplary implementation, the portion of silicon layer 130 not located below photoresist mask 140 may be etched in a conventional manner with the etching terminating on buried oxide layer 120, thereby forming fin 210, as illustrated in Fig. 2. Referring to Fig. 2, the fin 210 comprises silicon and may be formed to approximately the same width as photoresist mask 140 (e.g., a width of about 200 Å to about 500 Å).

[0030] After the formation of fin 210, source and drain regions may be formed adjacent respective ends of fin 210. For example, in an exemplary embodiment, a layer of silicon, germanium or combination of silicon and germanium may be deposited, patterned and etched in a conventional manner to form source and drain regions. Alternatively, silicon layer 130 may be patterned and etched to form source and drain regions.

[0031] Fig. 3 illustrates a top view of the semiconductor device 100 of Fig. 2 consistent with the present invention after the source and drain regions are formed. The cross-section illustrated in Fig. 2 is taken along line AA in Fig. 3. As illustrated in Fig. 3, semiconductor device 100 includes fin 210, source region 320 and drain region 330.

[0032] Next, the source region 320 and drain region 330 may be covered, for example, with a mask, as indicated by the cross-hatching illustrated in source/drain regions 320 and 330 in Fig. 4. The mask may be a hard mask comprising a silicon oxide, silicon nitride or some other material. The fin 210 may then be thinned.

[0033] For example, an isotropic etch may be performed to thin fin 210 in the channel region of semiconductor device 100, as illustrated in Fig. 5. Referring to Fig. 5, the dotted lines represent the width of fin 210 prior to the etching. In an exemplary embodiment, the width of fin 210 after the etching (represented by "W" in Fig. 5) may be as small about 50 Å to about 200 Å. Advantageously, the thin fin 210 enables semiconductor device 100 to achieve better short-channel control.

[0034] During the isotropic etching, the height or thickness of fin 210 in the vertical direction may also be reduced, as illustrated in Fig. 6. In an exemplary embodiment, the thickness of fin 210 in the vertical direction may be reduced by about 200 Å to about 400 Å during the etching. The resulting thickness of fin 210 in the vertical direction (represented by "H" in Fig. 6) may be as small as about 500 Å to about 800 Å.

[0035] The particular etch chemistry, gas flow rates, power ranges, bias voltages, etch duration and other parameters associated with etching fin 210 may be optimized based on the

thickness of fin 210 prior to the etching and the particular end device requirements. In an exemplary implementation, the isotropic etch of fin 210 may use a wet etch chemistry.

[0036] In addition, the mask formed over the source/drain areas 320 and 330 (illustrated in Fig. 4) may be removed via a conventional etching, thereby exposing the source/drain areas 320 and 330, as illustrated in Fig. 6. Alternatively, the hard mask may be left covering the source/drain areas 320 and 330.

[0037] A dielectric layer 710, such as a silicon oxide layer (e.g., SiO_2) or a silicon nitride layer (e.g., Si_3N_4), may be formed over fin 210, as illustrated in Fig. 7. Dielectric layer 710 may act as a gate dielectric for a subsequently formed gate and/or as a protective cap to protect the fin 210 during subsequent processing. In an exemplary implementation, dielectric layer 710 may be deposited or thermally grown on fin 210 to a thickness ranging from about 10 Å to about 20 Å. In alternative implementations, more than one dielectric layer may be formed over fin 210, such as an oxide layer with a nitride layer formed thereon.

[0038] A conductive layer may then be deposited to form a gate electrode. In an exemplary implementation, the conductive layer may include polysilicon deposited using conventional chemical vapor deposition (CVD) to a thickness ranging from about 300 Å to about 800 Å. Alternatively, other semiconducting materials, such as germanium or combinations of silicon and germanium, or various metals may be used as the gate material. The conductive layer may be patterned and etched to form a gate electrode 810, as illustrated in Fig. 8A.

[0039] Referring to Fig. 8A, the gate electrode 810 is formed over the fin 210 and gate dielectric 710 in the channel region of semiconductor device 100. The source and drain regions 320 and 330, respectively, are thicker in the vertical direction than fin 210, as illustrated in Fig. 8A. That is, source and drain regions 320 and 330 are effectively raised to a height above fin 210 in the vertical direction as a result of the isotropic thinning of fin 210 described above with respect to Figs. 5 and 6. In an exemplary implementation, the height or thickness of the

source/drain regions 320 and 330 may be at least 200 Å greater than the height or thickness of fin 210. For example, the height of the source/drain regions 320 and 330 may range from 700 Å to 1000 Å when the height of fin 210 ranges from 500 Å to 800 Å. Advantageously, the raised source/drain regions 320 and 330 can reduce source/drain series resistance and hence improve device drive current.

[0040] Fig. 8B illustrates a top view of semiconductor device 100 consistent with the present invention after the gate electrode 810 is formed. The cross section illustrated in Fig. 8A is taken along line BB in Fig. 8B. Referring to Fig. 8B, semiconductor device 100 includes a double gate structure with gate electrode 810 being disposed on either side of fin 210. The dielectric layer 710 (Fig. 7) above the upper surface of fin 210 is not shown in Fig. 8B for simplicity. Gate electrode 810 may include gate contacts 820 and 830 formed at the respective ends of gate electrode 810, as illustrated in Fig. 8B. The resulting semiconductor device 100 illustrated in Figs. 8A and 8B is a double-gate device with a gate electrode disposed on either side of fin 210.

[0041] The source/drain regions 320 and 330 may then be doped. For example, n-type or p-type impurities may be implanted in source/drain regions 320 and 330. The particular implantation dosages and energies may be selected based on the particular end device requirements. One of ordinary skill in this art would be able to optimize the source/drain implantation process based on the circuit requirements and such steps are not disclosed herein in order not to unduly obscure the thrust of the present invention. In addition, sidewall spacers may optionally be formed prior to the source/drain ion implantation to control the location of the source/drain junctions based on the particular circuit requirements. Activation annealing may then be performed to activate the source/drain regions 320 and 330.

[0042] Thus, in accordance with the present invention, a double-gate FinFET device is formed with a narrow fin and source/drain regions that are raised up in the vertical direction with respect to the fin. Advantageously, the resulting structure exhibits good short channel behavior,

reduces source/drain series resistance and improves device drive current. In addition, the present invention provides increased flexibility and can be easily integrated into conventional processing. Further, the present invention has been described with exemplary parameters associated with various parts of a semiconductor device 100, such as the exemplary thickness and width of fin 210 and the exemplary thickness of source/drain regions 320 and 330. It should be understood that these values are exemplary only and the actual thicknesses and width of these structures may be optimized based on the particular circuit requirements.

OTHER EXEMPLARY EMBODIMENTS

[0043] In some implementations, a FinFET may be formed with asymmetric gates. For example, semiconductor device 900 in Fig. 9A may include a buried oxide layer 905 formed on a substrate (not shown). Silicon fin 910 may be formed in a conventional manner, with gate dielectric 915 formed on the side surfaces of fin 910 and dielectric cap 920 formed over the top surface of the fin 910, as illustrated in Fig. 9A. The dielectric cap 920 may comprise a silicon nitride, a silicon oxide or another dielectric. Gate electrode 930 may be formed over fin 910 and may comprise polysilicon.

[0044] Fig. 9B illustrates the top view of the semiconductor device 900 of Fig. 9A. Referring to Fig. 9B, semiconductor device 900 includes source region 935 and drain region 940 disposed on either side of fin 910 and gate electrode 930 formed over fin 910.

[0045] A thick oxide layer 945 may be deposited over gate electrode 930 and polished to form a relatively flat surface, as illustrated in Fig. 9C. The polishing of oxide layer 945 may continue until polysilicon gate 930 and dielectric cap 920 are exposed, as illustrated in Fig. 9D. Fig. 9E illustrates a top view of semiconductor device 900 after dielectric cap 920 and gate electrode 930 are exposed. The cross-hatched areas in Fig. 9E located adjacent fin 910 represent the exposed portions of gate electrode 930.

[0046] A photoresist material 950 may then be deposited to cover one side of semiconductor device 900, as illustrated in Fig. 9F. The thickness of photoresist layer 950 may be about 100 nm. The photoresist layer 950 may cover a portion of the gate electrode 930 on one side of fin 910. For example, in Fig. 9F, photoresist layer 950 covers the left side of gate electrode 930. In an exemplary implementation, photoresist material 950 may also cover or overlay about 30 nm of the uncovered side of gate electrode 930 (i.e., the right side in Fig. 9F) and at least 40 nm of the uncovered side of gate electrode 930 will be exposed, as illustrated in Fig. 9F.

[0047] The exposed polysilicon in gate electrode layer 930 may then be etched via, for example, an isotropic etch. The etching may use, for example, HBr, and may be very selective to polysilicon. During the etching, the polysilicon in gate electrode 930 not located under the photoresist layer 950 may be removed, as illustrated in Fig. 9G. In addition, the small portion of polysilicon on the right side of gate electrode 930 in Fig. 9G located below photoresist layer 950 may also be removed (i.e., the portion under the overlaying part of photoresist layer 950).

[0048] The photoresist layer 950 may then be stripped and the polysilicon that has been removed may be replaced with polysilicon having a different dopant. For example, if polysilicon layer 930 was doped with n-type impurities, a polysilicon layer doped with p-type impurities may be deposited on the right side of fin 910. The polysilicon may be deposited via a chemical vapor deposition (CVD) process and may be patterned to form a gate electrode 955 on the right side of fin 910, as illustrated in Fig. 9H.

[0049] The resulting semiconductor device 900 is a double-gate device with a first gate electrode 930 and a second gate electrode 955. Since the gate electrodes 930 and 955 are asymmetrically doped, gates 930 and 955 may have different work functions. In addition, by varying the dopant concentrations, the threshold voltage of gate electrodes 930 and 955 may be independently adjusted based on the particular circuit requirements.

[0050] In an alternative implementation, asymmetric gates may be formed by an etchback of a damascene gate electrode. For example, semiconductor device 1000 of Fig. 10A includes a buried oxide layer 1005 formed on a substrate (not shown). Silicon fin 1010 may be formed on buried oxide layer 1005 and source region 1015 and drain region 1020 may be formed adjacent either side of fin 1005. A nitride layer 1025 may be formed over the upper surface of fin 1010 and source/drain regions 1015 and 1020, as illustrated in Fig. 10A. Fig. 10B illustrates a top view of semiconductor device 1000 of Fig. 10A. The nitride layer 1025 is not illustrated in Fig. 10A for simplicity.

[0051] A damascene gate electrode 1030 may then be formed as illustrated in Fig. 10C. The gate electrode 1030 may be planarized so that the top surface of the gate electrode 1030 is planar with nitride layer 1025. Fig. 10D illustrates a top view of semiconductor device 1000 of Fig. 10C. In some implementations, nitride layer 1025 may cover the center portion of fin 1010 and electrically separates one side of gate electrode 1030 from the other side of gate electrode 1030, as illustrated in Fig. 10D.

[0052] A photoresist mask 1040 may then be formed on one side of semiconductor device 1000, as illustrated in Fig. 10E. An isotropic poly etch may then be performed to remove the polysilicon in gate electrode 1030 not covered by mask 1040 (i.e., the bottom portion of gate electrode 1030 in Fig. 10E). For example, an isotropic etch using HBr or SF₆ may be used to remove the polysilicon in gate electrode 1030 not protected by mask 1040. Doped n-type or p-type polysilicon may then be deposited. For example, if gate electrode 1030 was doped with n-type impurities, a polysilicon layer doped with p-type impurities may be deposited and planarized to form a p-type doped polysilicon gate electrode. For example, the polysilicon may be deposited via a chemical vapor deposition (CVD) process and patterned to form gate electrode 1050, as illustrated in Fig. 10F. Alternatively, a metal may be deposited and polished to form a metal gate electrode 1050.

[0053] The resulting semiconductor device 1000 is a double-gate device with a first gate electrode 1030 and a second gate electrode 1050. The gates electrodes are electrically and physically separated by fin 1010. Each of the gate electrodes 1030 and 1050 may be separately biased. For example, gate electrode 1030 may be biased with a different voltage than gate electrode 1050 based on the particular circuit requirements. In addition, since the gate electrodes 1030 and 1050 are asymmetrically doped, the gates 1030 and 1050 will have different work functions. By varying the dopant concentrations, the threshold voltage of gate electrodes 1030 and 1050 may be independently adjusted based on the particular circuit requirements.

[0054] The embodiments illustrated in Figs. 9A-9H and 10A-10F enable the formation of asymmetric gates and/or independent gates without requiring independent patterning. The procedures are self-aligned and may be used with both conventional and damascene double-gate definition schemes.

[0055] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

[0056] The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of CVD processes, including low pressure CVD (LPCVD) and enhanced CVD (ECVD) can be employed.

[0057] The present invention is applicable in the manufacturing of double-gate semiconductor devices and particularly in FinFET devices with design features of 100 nm and below. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the

thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

[0058] In addition, no element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

[0059] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.